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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,807	02/29/2000	Richard B Merrill	FOV-036	1008

7590 04/22/2004

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EXAMINER	
YE, LIN	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/515,807	Applicant(s) MERRILL ET AL.	
	Examiner Lin Ye	Art Unit 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to amended claims 1-38 filed on 2/12/04 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments filed 2/12/04 have been fully considered but they are not persuasive as to claims 39-49.

Referring to claim 39, the examiner understands the applicant's specification and figures that show an exposure transistor having a source **directly connected** to a output of a source-follower transistor and drain **directly connected** to a global current-summing node. However, the claim only states "an exposure transistor having a source **coupled** to said output of said source-follower transistor and drain **coupled** to a global current-summing node". The means of "**coupled**" is broader than "**directly connected**" and only requires two elements connected in a circuit without excluding other elements between them. For that reason, It can be considered that the Wu reference discloses an exposure transistor (M4 in Figure 3) having a source coupled to said output of said source-follower transistor (M3) and drain coupled to a global current-summing node (VDD in Figure 3), said exposure transistor having a control gate coupled to a saturation level (WL signal) control voltage (See Col. 2, lines 40-44).

Claim Objections

3. Applicant is advised that should claim 30 be found allowable, claim 38 will be objected to under 37 CFR 1.75 as being a substantial **duplicate** thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP 706.03(k).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-9, 11-19, 21-29 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Buhler et al. U.S. Patent 5,742,047.

Referring to claim 1, the Buhler reference discloses in Figure 1, a plurality of storage pixel sensors (CMOS sensor array, see Col. 3, lines 5-10) disposed on a semiconductor substrate, each of the plurality of storage pixel sensors comprising: a photodiode (D1) having a first terminal coupled to a first potential and a second terminal; a reset transistor (M1) having a first terminal coupled to the second terminal of the photodiode, a second terminal coupled to a reset reference potential that reverse biases the photodiode (See Col. 3, lines 11-16), and a control gate coupled to a RESET signal node (ϕDR); a photocharge integration node (C1) coupled to said first terminal of said reset transistor (M1), said photocharge

integration node comprising the control gate of a source follower transistor (M4), said source-follower transistor having a drain, coupled to a source follower drain supply voltage node (VDD), and a source coupled to means for generating a bias current (bias transistor M5); and a capacitive storage node (C5), coupled to the source of the source-follower transistor (M4), comprising the input of a readout amplifier transistor (M11) having an output.

Referring to claim 2, the Buhler reference discloses including means for selectively pulsing (VDD signal) said source-follower drain supply voltage node (See Col. 3, lines 20-30).

Referring to claim 3, the Buhler reference discloses wherein said readout amplifier (M11) is a second source-follower transistor having a drain coupled to a second source-follower drain supply voltage (VDD) node and said capacitive storage node (node 24 of C5) is a gate associated therewith as shown in Figure 1.

Referring to claim 4, the Buhler reference discloses wherein further coupled to means for selectively pulsing (VDD) said second source-follower drain supply voltage (See Col. 4, lines 1-8).

Referring to claim 5 the Buhler reference wherein said means for generating a bias current comprises a bias transistor (bias transistor M5) having a source coupled to a fixed voltage source, a gate coupled to a bias voltage (VDD) node and a drain coupled to the source of said source follower transistor (M4).

Referring to claim 6, the Buhler reference discloses wherein the gate of said bias transistor (M5) is coupled to a bias voltage (VDD) node that may be selectively pulsed (VDD signal, see Col. 3, lines 31-40).

Referring to claim 7, the Buhler reference discloses wherein further including a barrier transistor (M2) having first and second terminals coupled between the second terminal of the photodiode (D1) and said first terminal of said reset transistor (M1), said barrier transistor (M2) having a control terminal (VT1) coupled to a barrier set voltage.

Referring to claim 8, the Buhler reference wherein said reset transistor (M1) and said barrier transistor (M2) are sized so as to have substantially matched voltage thresholds (See Col. 3, lines 14-22).

Referring to claim 9, the Buhler reference wherein a transfer transistor (M10) disposed between said source of said source-follower transistor (M4) and the capacitive storage node (node 24 of C5), said transfer transistor (M10) having a first terminal coupled to said source of said source-follower transistor, a second terminal coupled to the capacitive storage node and a control gate coupled to a XFR signal (ΦS/H signal) node (See Col. 3, lines 64-67).

Referring to claim 11, the Buhler reference wherein an exposure transistor (M9) having a source coupled to said output of said source-follower transistor (M4) and drain coupled to a global current-summing node (V4.5), said exposure transistor having a control gate coupled to a saturation level control voltage (ΦC).

Referring to claim 12, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claims 1 and 7.

Referring to claim 13, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 2.

Referring to claim 14, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 3.

Referring to claim 15, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 4.

Referring to claim 16, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 5.

Referring to claim 17, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 6.

Referring to claim 18, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 8.

Referring to claim 19, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 9.

Referring to claim 21, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 11.

Referring to claim 22, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claims 1 and 11.

Referring to claim 23, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 2.

Referring to claim 24, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 3.

Referring to claim 25, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 4.

Referring to claim 26, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 5.

Referring to claim 27, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 6.

Referring to claim 28, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 8.

Referring to claim 29, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claim 9.

Referring to claim 31, the Buhler reference discloses all subject matter as discussed with respected to same comment as with claims 1 and 9.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 39-49 are rejected under 35 U.S.C. 102(e) as being anticipated by Wu et al. U.S. Patent 6,111,245.

Referring to claim 39, Referring to claim 1, the Wu reference discloses in Figures 2-3 and 5, a storage pixel sensor disposed on a semiconductor substrate comprising: a photodiode (D2) having a first terminal coupled to a first potential and a second terminal; a reset transistor (M2 in Figure 3) having a first terminal coupled to the second terminal of the photodiode, a second terminal coupled to a reset reference potential that reverse biases the photodiode (See Col. 2, lines 19-23), and a control gate coupled to a RESET signal node; a photocharge integration node (point b in Figure 3) coupled to said first terminal of said reset transistor (M2), said photocharge integration node comprising the control gate of a source follower transistor (M3), said source-follower transistor having a drain, coupled to a source follower drain supply voltage node, and a source coupled to means for generating a bias current (bias transistor M5); and an exposure transistor (M4 in Figure 3) having a source coupled to said output of said source-follower transistor (M3) and drain coupled to a global current-summing node (VDD in Figure 3), said exposure transistor having a control gate coupled to a saturation level (WL signal) control voltage (See Col. 2, lines 40-44).

Referring to claim 40, the Wu reference discloses including means for selectively pulsing (VDD signal) said source-follower drain supply voltage node.

Referring to claim 41, the Wu reference discloses wherein said means for generating a bias current comprises a bias transistor (bias transistor M5 in Figure 3) having a source coupled to a fixed voltage source, a gate coupled to a bias voltage (Vb) node and a drain coupled to the source of said source follower transistor (M3 in Figure 3).

Referring to claim 42, the Wu reference discloses wherein the gate of said bias transistor (M5 in Figure 3) is coupled to a bias voltage (Vb) node that may be selectively pulsed (Vb signal).

Referring to claim 43, the Wu reference discloses wherein further including a barrier transistor (M1 in Figure 3) having first and second terminals coupled between the second terminal of the photodiode (D2 in Figure 3) and said first terminal of said reset transistor (M2 in Figure 3), said barrier transistor having a control terminal (Shutter in Figure 3) coupled to a barrier set voltage (see Col. 2, lines 60-65).

Referring to claim 44, the Wu reference discloses wherein said reset transistor (M2 in Figure 3) and said barrier transistor (M1 in Figure 3) are sized so as to have substantially matched voltage thresholds (See Col. 3, lines 1-22).

Referring to claim 45, the Wu reference discloses a capacitive storage node (point C in Figure 5), coupled to the source of the source-follower transistor (M3 in Figure 3), comprising the input of a readout amplifier transistor having an output as shown in Figure 3.

Referring to claim 46, the Wu reference discloses wherein said readout amplifier (M1 in Figure 5) is a second source-follower transistor having a drain coupled to a second source-follower drain supply voltage (VSS in Figure 5) node and said capacitive storage node (point c) is a gate associated therewith..

Referring to claim 47, the Wu reference discloses wherein further coupled to means for selectively pulsing (VDD signal in Figure 5) said second source-follower drain supply voltage.

. Referring to claim 48, the Wu reference discloses wherein a transfer transistor disposed between said source of said source-follower transistor (M3 in Figure 3) and the capacitive storage node (point c), said transfer transistor (having a first terminal coupled to said source of said source-follower transistor, a second terminal coupled to the capacitive storage node and a control gate coupled to a XFR signal (Φ1 signal) node (See Col. 3, lines 46-51).

Referring to claim 49, the Wu reference discloses wherein row-select transistor (M2 in Figure 5) having a first terminal coupled to the output of the readout amplifier (M1 in Figure 5), a second terminal coupled to a column output line (Vout line) and a control gate coupled to a ROW SELECT signal (Ysel signal used to output the signal on same line) node; and a control circuit (row decoder 22 and column decoder 23 in Figure 2) for selectively activating a RESET signal (CK, M4 and M5 are commonly used by many lines for providing a reset voltage in Figure 5) on said RESET signal node, a XFR signal (Φ1 signal) on said XFR signal node, and a ROW SELECT (Ysel) signal on said ROW SELECT signal node as shown in Figure 6 (See Col.3, lines 30-62).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 10, 20, 30 and 32-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buhler et al. U.S. Patent 5,742,047 in view of Wu et al. U.S. Patent 6,111,245.

Referring to claim 10, the Buhler reference discloses all subject matter as discussed in respected claims 1 and 9, except the reference does not has a detail to show the two dimensional sensor array circuit including a row decoder to control row select signal for each of rows and a row-select transistor in each of pixel sensors.

The Wu reference discloses in Figures 2-3 and 5, a row-select transistor (M12) having a first terminal coupled to the output of the readout amplifier (M11), a second terminal coupled to a column output line (output node 26) and a control gate coupled to a ROW SELECT signal (VDD) node; and a control circuit (row decoder 22 and column decoder 23 in Figure 2) for selectively activating a RESET signal (CK, M4 and M5 are commonly used by many lines for providing a reset voltage in Figure 5) on said RESET signal node, a XFR signal (Φ1 signal) on said XFR signal node, and a ROW SELECT (Ysel) signal on said ROW SELECT signal node as shown in Figure 6 (See Col.3, lines 30-62). The Wu reference is evidence that one of ordinary skill in the art at the time to see more advantages each of pixel sensors in the sensor array including a row select transistor for receiving a row select signal from the row decoder control circuit in order readout image signal line by line to column output line. For that reason, it would have been obvious to a row-select transistor having a first terminal coupled to the output of the readout amplifier, a second terminal coupled to a column output line and a control gate coupled to a ROW SELECT signal node and a ROW select signal on said ROW SELECT signal node disclosed by Buhler.

Referring to claim 20, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 10.

Referring to claim 30, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 10.

Referring to claim 32, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 2 and 30.

Referring to claim 33, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 3 and 30.

Referring to claim 34, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claims 4 and 30.

Referring to claim 35, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 5 and 30.

Referring to claim 36, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 6 and 30.

Referring to claim 37, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 8 and 30.

Referring to claim 38, the Buhler and Wu reference disclose all subject matter as discussed with respected to same comment as with claim 10.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Lin Ye** whose telephone number is **(703) 305-3250**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, DC. 20231

Or faxed to:

(703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Lin Ye
April 13, 2004